What are the steps, in order, to fix a “simulator-is-wedged” problem?

Stop the current simulation then start it again. You may have to close and reopen Vivado. Make sure that only one instance of Vivado is running. Check the task manager to see if there are other instances open. Enable Incremental Compilation in the simulation settings. Clear the cache by deleting all the sv and tcl files but not the project files.

Attach a PDF file of your Tcl file commands to LearningSuite. You can create such a PDF file from the File->Print menu in Vivado while editing it.

Attach a screenshot of your simulation results that show how your circuit works as intended. In order to receive full credit on this (and all simulations for the rest of the semester), you MUST describe in detail in words in the LearningSuite response box for this question, how you went out verifying that it works. Point out the important time places in the simulation, what was happening there, what the inputs were, what the outputs were, and why they are the correct outputs, etc.

On the sv file, I specified the four different functions using the parameters of A, B, and C to get the outputs of O1 to O4. The first function is usually true unless C isn’t true. This is because it doesn’t really matter what A is because of the or but it matters what the other two are. The second function is only true when all three are true. This is because C has to be true in combination with B and A has to be true as well to satisfy the or on the left side is C is already true. The 3rd function is always true if C is true because of the last or gate. It can also be true if only A is true to satisfy the and gate on the top. The fourth function is usually true if A is true because the top and gate will be false then notted causing the last gate to be false and the final output notted to true. This only doesn’t work when C is true with A true because it will cause a similar situation on the bottom nand gate causing the final nand gate to be true then notted to false. The last working function is if everything starts false as the top nand gate outputs true while the bottom outputs false.

I had 2 errors that simply said that I had some redundant code. I declared the variables notB and notC twice since they were used in different functions. I deleted the repeated code because they would have created the same output as they did in the earlier functions.

Summarize some of the differences between the schematic you captured earlier and the synthesis schematic

The first schematic had the actions of every single gate created while completely translated the sv file created. The synthesis schematic was much simpler and had the final outputs of every variable without displaying every gate they went through. It was simpler to see which outputs they ended up in but not which gates may have caused problems.

LUT - 2

IO - 7